Christian Pilato

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Education

- **Ph.D. in Information Technology** at Politecnico di Milano *Feb. 2011*
  Thesis Title: *Design Methodologies for Improving Embedded Systems with Hardware Accelerators*
  Advisor: *Fabrizio Ferrandi – Donatella Sciuto*
- **M.Sc. in Computer Science Engineering** at Politecnico di Milano *Apr. 2007*
  Thesis title: *High-Level Synthesis with Area Constraints for FPGA Designs: An Evolutionary Approach*
  Advisor: *Fabrizio Ferrandi* – Grade: 110/110

Research Experience

- **Associate Professor** *Mar. 2023* – current
  Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Italy
  – High-level synthesis for hardware security; design of heterogeneous architectures; high-performance computing and big data analytics; machine learning and generative AI to enhance augmentative and alternative communication.
- **Senior Assistant Professor (RTD-B)** *Mar. 2020 – Mar. 2023*
  Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Italy
  – High-level synthesis for hardware security; design of heterogeneous System-on-Chip architectures.
- **Junior Assistant Professor (RTD-A)** *Jun. 2018* – Feb. 2020
  Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Italy
  – High-level synthesis for hardware security; design of heterogeneous System-on-Chip architectures.
- **Research Fellow** *Sept. 2017 – May 2018*
  Center of Cybersecurity, New York University, USA (*Ramesh Karri and Siddharth Garg*)
  – High-level synthesis for hardware security.
- **Postdoctoral Researcher** *Feb. 2017 – May 2018*
  Faculty of Informatics, Università della Svizzera italiana, Switzerland (*Francesco Regazzoni*)
  – Design methodologies for security-aware high-level synthesis, security metrics for cyber-physical systems.
- **Visiting Research Scientist** *Sept. 2016 – Jan. 2017*
  Department of Microelectronics, Delft University of Technology, The Netherlands (*Edoardo Charbon*)
  – Design of FPGA controllers for SPAD chips.
- **Visiting Research Scientist** *Jun. 2016 – Aug. 2016*
  Faculty of Informatics, Università della Svizzera italiana, Switzerland (*Francesco Regazzoni*)
  – Design methodologies for security-aware heterogeneous architectures.
- **Postdoc Research Scientist** *Sept. 2013 – May 2016*
  Department of Computer Science, Columbia University, USA (*Luca P. Carloni*)
  – Design and integration of hardware accelerators for heterogeneous architectures (including FPGA prototypes, CPU-FPGA platforms, and SoCs), with emphasis on memory-related aspects.
- **Postdoc Research Assistant** *Jun. 2011 – Sept. 2013*
  Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Italy (*Donatella Sciuto*)
  – Hardware-software methodologies for the design of partially reconfigurable architectures.
- **Visiting Researcher** *Sept. 2012 – Dec. 2012*
  Department of Computer Science, Chalmers University of Technology, Sweden (*Georgi Gaydadjiev*)
  – Integration of polymorphic register files for high-performance dataflow computing.

- **Visiting Researcher** *Dec. 2009 – May 2010*
  Nangate A/S, Denmark (*Martin Elhøj*)
  – Design of application-specific standard-cell libraries to improve circuit manufacturing.
- **Research Assistant** *Jun. 2007 – Dec. 2007*
  Dipartimento di Elettronica ed Informazione, Politecnico di Milano, Italy (*Donatella Sciuto*)
  – Development of hardware-software co-design methods for heterogeneous architectures.

Qualifications

- **Italian National Scientific Qualification** *Jun. 2018*
  Habilitation to the function of *Associate Professor* in *Information Processing Systems* (Sector: 09/H1).
- **Italian National Engineering License** *2008*
  Professional practice examination in *Computer Engineering*.

Awards and Honors

- **Best Paper Award** for the paper "Using Static Analysis for Enhancing HLS Security", presented at the *HiPEAC Workshop on Secure Hardware, Architectures, and Software* (SeHAS 2024)
- HiPEAC Award for the paper "ALICE: An Automatic Design Flow for eFPGA Redaction" published at the *ACM/IEEE Design Automation Conference* (DAC 2022)
- HiPEAC Award for the paper "Designing ML-Resilient Locking at Register-Transfer Level" published at the *ACM/IEEE Design Automation Conference* (DAC 2022)
- HiPEAC Award for the paper "Invited: High-level design methods for hardware security: Is it the right choice?" published at the *ACM/IEEE Design Automation Conference* (DAC 2022)
- HiPEAC Award for the paper "Invited: Bambu: an Open-Source Research Framework for the High-Level Synthesis of Complex Applications" published at the *ACM/IEEE Design Automation Conference* (DAC 2021)
- HiPEAC Award for the paper "Fortifying RTL Locking Against Oracle-Less (Untrusted Foundry) and Oracle-Guided Attacks" published at the *ACM/IEEE Design Automation Conference* (DAC 2021)
- HiPEAC Award for the paper "TAO: Techniques for Algorithm-Level Obfuscation during High-Level Synthesis" published at the *ACM/IEEE Design Automation Conference* (DAC 2018)
- Collaboration grant (5K€) by HiPEAC European Network of Excellence for the research "Adaptive and heterogeneous computing systems" with Chalmers University of Technology, Gothenburg, Sweden (2012)
- Ph.D. fully funded by a scholarship from STMicroelectronics (2008–2010)

Research Projects

Scientific Committees

Dr. Pilato contributed to the following scientific committees:

- Reviewer for the Swiss National Science Foundation (SNSF), (2020, 2023)
- Panel Member for the NSF Graduate Research Fellowship Program (GRFP), (2016)

Positions of Trust

Dr. Pilato is currently leading the following grants:

- *EVEREST (dEsign enVironmEnt foR Extreme-Scale big data analyTics on heterogeneous platforms)*, EU H2020 PROJECT, CONTRACT NO. 957269
  Total budget ∼5M€, PI funding amount: ∼650K€
  Dr. Pilato is the **Scientific Coordinator** of the project and the **Principal Investigator** for Politecnico di Milano. EVEREST consortium includes ten partners from six countries: IBM Research Zurich and Università della Svizzera italiana (Switzerland), Politecnico di Milano, Centro Internazionale in Monitoraggio Ambientale, and Duferco (Italy), Technical University of Dresden (Germany), Virtual Open Systems and Numtech (France), IT4Innovations (Czech Republic), and Sygic (Slovakia). The EVEREST project aims at developing a design environment (i.e., compilation framework and runtime environment) for extreme Big Data applications on heterogeneous platforms.

Dr. Pilato took a prominent role in the following research projects:

- *RTL Obfuscation Deployment and Evaluation*, DARPA TRUSTED SILICON STRATUS (TSS) PROGRAM (2020)
  PI funding amount: $35K, ∼30K€
  Dr. Pilato was the **Principal Investigator** for Politecnico di Milano in a subcontract with New York University (NYU) and the Boeing Company for the evaluation of RTL obfuscation techniques within the Nimbus cloud environment.
- *FASTER (Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration)*, EU FP7 SPECIFIC TARGETED RESEARCH PROJECT (STREP), CONTRACT NO. 287804 (2011-2013)
  Local project leader: Donatella Sciuto, Politecnico di Milano.
  Dr. Pilato was the **Task Leader** of "Application Task Profiling and Identification of Reconfigurable Cores", which included the work of FORTH (Greece), Chalmers University of Technology (Sweden), Imperial College (UK), Politecnico di Milano (Italy), and Ghent University (Belgium). This task defined design methodologies for reconfigurable systems, involving the concurrent definition of the architecture (i.e., feasible reconfigurable regions) and the application (i.e., corresponding hardware-software partitioning). He collaborated with the local leader and the project coordinator since the definition of the proposal, providing support for all managerial aspects.

Project Participation

In the past, he contributed to the following research projects:

- DARPA CIRCUIT REALIZATION AT FASTER TIMESCALES (CRAFT) PROGRAM
  Local project leaders: Siddharth Garg and Ramesh Karri, New York University (NYU), Steve Fisher (Boeing)
  Dr. Pilato was an NYU external consultant for the definition of high-level design methodologies to obfuscate digital circuits and prevent reverse engineering of the chips to be fabricated. The results of this research produced a tool-flow that has been used to design an obfuscated chip later fabricated at 16nm.
- *CERBERO (Cross-layer modEl-based fRamework for multi-oBjective dEsign of Reconfigurable systems in unceRtain hybRid envirOnments)*, EU H2020 PROJECT, CONTRACT NO. 732105
  Local project leader: Francesco Regazzoni, Università della Svizzera italiana (USI Lugano).
  Dr. Pilato worked on performance indicators and design methodologies to incorporate security concepts into the design of reliable and adaptive cyber-physical systems. This work was mainly done in collaboration with University of Sassari, University of Cagliari, Thales Alenia Space, Centro Ricerche Fiat, Polytechnic University of Madrid, Netherlands Organisation for Applied Scientific Research (TNO), and IBM Haifa.
- *C-FAR (Center for Future Architectures Research)*, STARNET RESEARCH CENTER
  Local project leader: Luca Carloni, Columbia University.
  Dr. Pilato worked on design methodologies and CAD tools for the optimization of the accelerator local memory in heterogeneous SoCs. This also included hardware support for the allocation of massive data sets.
- *ESP (Embedded Scalable Platform)*, DARPA POWER EFFICIENCY REVOLUTION FOR EMBEDDED COMPUTING TECHNOLOGIES (PERFECT) PROJECT, CONTRACT NO. HR0011-13-C-0003
  Local project leader: Luca Carloni, Columbia University.
  Dr. Pilato provided support for the FPGA prototype of the proposed SoC architecture. His work includes the support for the integration of hardware accelerators, the exploration of multiple design implementations, and the characterization of the power consumption for the different components at each voltage-frequency pair. This work has been mainly done in collaboration with the *Bioelectronics Systems* lab at Columbia University (Ken Shepard).
- *Synaptic (SYNthesis using Advanced Process Technology Integrated in regular Cells, IPs, architectures, and design platforms)*, EU FP7 SPECIFIC TARGETED RESEARCH PROJECT (STREP), CONTRACT NO. 248538
  Local project leader: Fabrizio Ferrandi, Politecnico di Milano.
  Dr. Pilato defined a heuristic methodology to automatically identify a minimal set of application-specific standard cells to extend an existing library and improve the manufacturing of digital circuits in state-of-the-art industrial flows. He also provided support through all project's phases since the definition of the proposal.
- *hArtes (Holistic Approach to Reconfigurable real Time Embedded Systems)*, EU FP6 INTEGRATED PROJECT (IP), CONTRACT NO. 035143
  Local project leader: Donatella Sciuto, Politecnico di Milano.
  Dr. Pilato was involved in the definition of compiler-based methodologies (based on GCC) for the semi-automatic parallelization of sequential C-based applications. He also proposed methodologies for defining an early hardware-

software partitioning in heterogeneous architectures having limited hardware resources and multiple hardware implementations generated with the support of high-level synthesis.

Complete List of Scientific Publications

Publication Summary

JR	Refereed international journals	26
IC	Refereed international conferences	60
BC	Refereed chapters in international books	6
WS	Refereed workshops with formal proceedings	12
	TOTAL	**104**
ED	Editorial contributions	5
WI	Workshops with informal proceedings	9
OA	Open-access publications and pre-prints	1

Metrics

Source	Citations	H-Index	Source	Citations	H-Index
Google Scholar	2,687	25	Scopus	1,528	19

Open-Access Publications

OA.1. A. Di Paola, S. Muraro, R. Marinelli, C. Pilato, "Foundation Models in Augmentative and Alternative Communication: Opportunities and Challenges," (*available from January 18, 2024*).
[arXiv: https://arxiv.org/abs/2401.08866]

Refereed Journal Publications

JR.26. L. Collini, J. Ah-kiow, C. Pilato, R. Karri, B. Tan, "Using Static Analysis for Enhancing HLS Security," in *IEEE Embedded Systems Letter*, (accepted October 24, 2023)
[Presented at the HiPEAC'24 workshop on "Secure Hardware, Architectures, and Software" (SeHAS 2024) - **Best Paper Award**]
[doi: http://doi.org/10.1109/LES.2023.3329417]

JR.25. R. Murillo, A. A. Del Barrio, G. Botella, C. Pilato, "Generating Posit-based Accelerators with High-Level Synthesis," in *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)*, vol. 70, no. 10, pp. 4040-4052, October 2023.
[doi: https://doi.org/10.1109/TCSI.2023.3299009]

JR.24. J. Bhandari, A. K. Thalakkattu Moosa, B. Tan, C. Pilato, G. Gore, X. Tang, S. Temple, P.-E. Gaillardon, R. Karri, "Not All Fabrics Are Created Equal: Exploring eFPGA Parameters For IP Redaction," in *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 31, no. 10, pp. 1459-1471, October 2023.
[doi: https://doi.org/10.1109/TVLSI.2023.3301334][arXiv: http://arxiv.org/abs/2111.04222]

JR.23. M. Tibaldi, C. Pilato, "A Survey of FPGA Optimization Methods for Data Center Energy Efficiency," in *IEEE Transactions on Sustainable Computing (TSUSC)*, vol. 8, no. 3, pp. 343-362, July-September 2023.
[doi: https://doi.org/10.1109/TSUSC.2023.3273852][arXiv: http://arxiv.org/abs/2309.12884]

JR.22. S. Soldavini, K. F. A. Friebel, M. Tibaldi, G. Hempel, J. Castrillon, C. Pilato, "Automatic Creation of High-Bandwidth Memory Architectures from Domain-Specific Languages: The Case of Computational Fluid Dynamics," in *ACM Transactions on Transactions on Reconfigurable Technology and Systems (TRETS)*, vol. 16, no. 2, pp. 1-34, June 2023.
[doi: https://doi.org/10.1145/3563553][arXiv: http://arxiv.org/abs/2111.04222]

JR.21. C. Pilato, L. Collini, L. Cassano, D. Sciuto, S. Garg, R. Karri, "Optimizing the Use of Behavioral Locking for High-Level Synthesis," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 42, no. 2, pp. 462-472, February 2023.
[doi: https://doi.org/10.1109/TCAD.2022.3179651][arXiv: http://arxiv.org/abs/2105.09666]

JR.20. M. Tibaldi, G. Palermo, C. Pilato, "Dynamically-Tunable Dataflow Architectures based on Markov Queuing Models," in *MDPI Electronics*, vol. 11, no. 5, February 2022.
[doi: https://doi.org/10.3390/electronics11040555]

JR.19. D. Parravicini, D. Conficconi, E. Del Sozzo, C. Pilato, M. D. Santambrogio, "CICERO: A Domain-Specific Architecture for Efficient Regular Expression Matching," in *ACM Transactions on Embedded Computing (TECS)* (*special issue on the papers presented at CASES 2021*), vol. 20, n. 5S, October 2021.
[doi: http://doi.org/10.1145/3476982]

JR.18. S. Soldavini, C. Pilato, "A Survey on Domain-Specific Memory Architectures," in *Journal of Integrated Circuits and Systems*, vol. 16, n. 2, August 2021.
[doi: http://dx.doi.org/10.29292/jics.v16i2.509][arXiv: http://arxiv.org/abs/2108.08672]

JR.17. C. Pilato, A. B. Chowdhury, D. Sciuto, S. Garg, R. Karri. "ASSURE: RTL Locking Against an Untrusted Foundry," in *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 29, no. 7, pp. 1306-1318, July 2021.
[doi: http://dx.doi.org/10.1109/TVLSI.2021.3074004][arXiv: http://arxiv.org/abs/2010.05344]

JR.16. M. Tibaldi, C. Pilato, F. Ferrandi. "Automatic Generation of Heterogeneous SoC Architectures with Secure Communications,", in *IEEE Embedded Systems Letter*, vol. 13, no. 2, pp. 61-64, June 2021.
[doi: http://dx.doi.org/10.1109/LES.2020.3003974]

JR.15. K. Basu, S.M. Saeed, C. Pilato, M. Ashraf, M.T. Nabeel, K. Chakrabarty, R. Karry. "CAD-Base: An Attack Vector into the Electronics Supply Chain," in *ACM Transactions on Design Automation of Electronics Systems (TODAES)*, vol. 24, no. 4, pp. 1-30, July 2019.
[doi: http://dx.doi.org/10.1145/3315574]

JR.14. C. Pilato, K. Wu, S. Garg, R. Karri, F. Regazzoni. "TaintHLS: Enabling Dynamic Information Flow Tracking in Hardware Accelerators," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 38, no. 5, pp. 798-808, May 2019.
[doi: http://dx.doi.org/10.1109/TCAD.2018.2834421]

JR.13. C. Pilato, K. Basu, F. Regazzoni, R. Karri. "Black-Hat High-Level Synthesis: Myth or Reality?," in *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 27, no. 4, pp. 913-926, April 2019.
[doi: http://dx.doi.org/10.1109/TVLSI.2018.2884742]

JR.12. C. Ciobanu, C. Pilato, G. Gaydadjiev, D. Sciuto. "The Case for Polymorphic Registers in Dataflow Computing," in *International Journal of Parallel Programming*, vol. 46, no. 6, pp. 1185–1219, December 2018.
[doi: http://dx.doi.org/10.1007/s10766-017-0494-1]

JR.11. P. Fezzardi, C. Pilato, F. Ferrandi. "Enabling Automated Bug Detection for IP-based Designs using High-Level Synthesis," in *IEEE Design & Test Magazine*, , vol. 35, no. 5, pp. 54-62, October 2018.
[doi: http://dx.doi.org/10.1109/MDAT.2018.2824121]

JR.10. C. Pilato, S. Garg, K. Wu, R. Karri, F. Regazzoni. "Securing Hardware Accelerators: a New Challenge for High-Level Synthesis," in *IEEE Embedded Systems Letter*, vol. 10, no. 3, pp. 77–80, September 2018.
[doi: http://dx.doi.org/10.1109/LES.2017.2774800]

JR.9. C. Pilato, P. Mantovani, G. Di Guglielmo, L.P. Carloni. "System-Level Optimization of Accelerator Local Memory for Heterogeneous Systems-on-Chip," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 36, no. 3, pp. 435–448, March 2017.
[doi: http://dx.doi.org/10.1109/TCAD.2016.2611506]

JR.8. R. Nane, V.-M. Sima, C. Pilato, J. Choi, B. Fort, A. Canis, Y.T. Chen, H. Hsiao, S. Brown, F, Ferrandi, J. Anderson, K. Bertels. "A Survey and Evaluation of FPGA High-Level Synthesis Tools," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 35, no. 10, pp. 1591–1604, October 2016.
[doi: http://dx.doi.org/10.1109/TCAD.2015.2513673]

JR.7. M. Lattuada, C. Pilato, F. Ferrandi. "Performance Estimation of Task Graphs based on Path Profiling," in *International Journal of Parallel Programming*, vol. 44, no. 4, pp. 735–771, August 2016.
[doi: http://dx.doi.org/10.1007/s10766-015-0372-7]

JR.6. D. Pnevmatikatos, K. Papadimitriou, T. Becker, P. Böhm, A. Brokalakis, K. Bruneel, C. Ciobanu, T. Davidson, G. Gaydadjiev, K. Heyse, W. Luk, X. Niu, I. Papaefstathiou, D. Pau, O. Pell, C. Pilato, M.D. Santambrogio, D. Sciuto, D. Stroobandt, T. Todman, E. Vansteenkiste. "FASTER: Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration," in *Microprocessors and Microsystems*, vol. 39, no. 4–5, pp. 321–338, June-July 2015.
[doi: http://dx.doi.org/10.1016/j.micpro.2014.09.006]

JR.5. A. Miele, C. Pilato, D. Sciuto. "A Simulation-based Framework for the Exploration of Mapping Solutions on Heterogeneous MPSoCs," in *International Journal of Embedded and Real-Time Communication Systems*, vol. 4, no. 1, pp. 22–41, April 2013.
[doi: http://dx.doi.org/10.4018/jertcs.2013010102]

JR.4. S. Cecchi, A. Primavera, F. Piazza, F. Bettarelli, E. Ciavattini, R. Toppi, J.G.F. Coutinho, W. Luk, C. Pilato, F. Ferrandi, V.M. Sima, K. Bertels. "The hArtes CarLab: A new approach to advanced algorithms development for automotive audio," in *Journal of the Audio Engineering Society*, vol. 59, no. 11, pp. 858–869, November 2011.
[url: http://www.aes.org/e-lib/browse.cfm?elib=16153]

JR.3. K. Bertels, V.M. Sima, Y. Yankova, G. Kuzmanov, W. Luk, J.G.F. Coutinho, F. Ferrandi, C. Pilato, M. Lattuada, D. Sciuto, A. Michelotti. "hArtes: Hardware-Software Codesign for Heterogeneous Multicore Platforms," in *IEEE Micro*, vol. 30, no. 5, pp. 88–97, September 2010.
[doi: http://dx.doi.org/10.1109/MM.2010.91]

JR.2. F. Ferrandi, P.L. Lanzi, C. Pilato, D. Sciuto, A. Tumeo. "Ant Colony Heuristic for Mapping and Scheduling Task and Communications on Heterogeneous Embedded Systems," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 29, no. 6, pp. 911–924, June 2010.
[doi: http://dx.doi.org/10.1109/TCAD.2010.2048354]

JR.1. C. Pilato, A. Tumeo, G. Palermo, F. Ferrandi, P.L. Lanzi, D. Sciuto. "Improving Evolutionary Exploration to Area-Time Optimization of FPGA Designs," in *Journal of Systems Architecture*, vol. 54, no. 11, pp. 1046–1057, November 2008.
[doi: http://dx.doi.org/10.1016/j.sysarc.2008.04.010]

Editorial contributions

ED.5. C. Pilato, P. Trancoso. "Message from the Program Chairs," in *Proceedings of the 41st IEEE International Conference on Computer Design (ICCD)*, November 2023.
[doi: http://doi.org/10.1109/ICCD58817.2023.00006]

ED.4. A. Awad, C. Pilato. "Message from the Program Chairs," in *Proceedings of the 40th IEEE International Conference on Computer Design (ICCD)*, October 2022.
[doi: http://doi.org/10.1109/ICCD56317.2022.00006]

ED.3. C. Pilato, Z. Fang, Y. Hara-Azumi, J. Hwang. "Introduction to the Special Section on High-Level Synthesis for FPGA: Next-Generation Technologies and Applications," in *ACM Transactions on Design Automation of Electronic Systems*, vol. 27, no. 4, July 2022.
[doi: http://dx.doi.org/10.1145/3519279]

ED.2. S. Vinco, C. Pilato. "Editorial: Special Issue on Innovative Design Methods for Smart Embedded Systems," in *ACM Transactions on Embedded Computing Systems*, vol. 15, no. 2, April 2016.
[doi: http://dx.doi.org/10.1145/2885505]

ED.1. C. Pilato, M. Porrmann. "Message from the Program Committee Chairs - EUC 2014," in *Proceedings of the 12th IEEE International Conference on Embedded and Ubiquitous Computing (EUC)*, September 2014.
[doi: http://doi.org/10.1109/EUC.2014.6]

Refereed Conference Publications

IC.60. C. Pilato, A. Di Paola, S. Muraro, R. Marinelli, "Using Artificial Intelligence to Boost Autonomy in a More Inclusive Society: The AMBRA Approach," in *3rd Third International Conference of the journal "Scuola Democratica"*, Cagliari, Italy, June 3-6, 2024.

IC.59. C. Pilato, S. Banik, J. Beranek, F. Brocheton, J. Castrillon, R. Cevasco, R. Cmar, S. Curzel, F. Ferrandi, K. Friebel, A. Galizia, M. Grasso, P. Guimaraes da Silva, J. Martinovic, G. Palermo, M. Paolino, A. Parodi, A. Parodi, F. Pintus, R. Polig, D. Poulet, F. Regazzoni, B. Ringlein, R. Rocco, K. Slaninova, T. Slooff, S. Soldavini, F. Suchert, M. Tibaldi, B. Weiss, C. Hagleitner, "A System Development Kit for Big Data Applications on FPGA-based Clusters: The EVEREST Approach," in *Proceedings of IEEE Design, Automation & Test in Europe Conference* (DATE 2024), Valencia, Spain, March 25-27, 2024, pp. 1-6.
[doi: (n.a.)][arXiv: https://arxiv.org/abs/2402.12612]

IC.58. C. Lu, C. Pilato, K. Basu, "Towards High-Level Synthesis of Quantum Circuits," in *Proceedings of IEEE Design, Automation & Test in Europe Conference* (DATE 2023), Antwerp, Belgium, April 17-19, 2023, pp. 1-6.
[doi: https://doi.org/10.23919/DATE56975.2023.10137010]

IC.57. S. Soldavini, D. Sciuto, C. Pilato, "Iris: Automatic Generation of Efficient Data Layouts for High Bandwidth Utilization," in *Proceedings of Asia and South Pacific Design Automation Conference* (ASPDAC 2023), pp. 1-6.
[doi: https://doi.org/10.1145/3566097.3567892][arXiv: https://arxiv.org/abs/2211.04361]

IC.56. L. Collini, B. Tan, C. Pilato, R. Karri, "Reconfigurable Logic for Hardware IP Protection: Opportunities and Challenges," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design* (ICCAD 2022), pp. 1-7.
[doi: https://doi.org/10.1145/3508352.3561117]

IC.55. C. Pilato, "High-Level Methods for Hardware IP Protections: Solutions, Trends, and Challenges," in *IEEE Dallas Circuits and Systems Conference* (DCAS 2022), pp. 1-2.
[doi: https://doi.org/10.1109/DCAS53974.2022.9845667]

IC.54. C. Pilato, D. Sciuto, S. Garg, R. Karri, "Invited: High-level design methods for hardware security: Is it the right choice?," in *ACM/IEEE Design Automation Conference* (DAC 2022), pp. 1-4.
[doi: https://doi.org/10.1145/3489517.3530635]

IC.53. D. Sisejkovic, L. Collini, J. Bhandari, B. Tan, R. Karri, C. Pilato, R. Leupers, "Designing ML-Resilient Locking at Register-Transfer Level," in *ACM/IEEE Design Automation Conference* (DAC 2022), pp. 1-6.
[doi: https://doi.org/10.1145/3489517.3530541][arXiv: https://arxiv.org/abs/2203.05399]

IC.52. C. Muscari Tomajoli, L. Collini, J. Bhandari, A. K. Thalakkattu Moosa, B. Tan, R. Karri, C. Pilato, "ALICE: An Automatic Design Flow for eFPGA Redaction," in *ACM/IEEE Design Automation Conference* (DAC 2022), pp. 1-6.
[doi: https://doi.org/10.1145/3489517.3530543][arXiv: https://arxiv.org/abs/2205.07425]

IC.51. G. Takhar, R. Karri, C. Pilato, S. Roy, "HOLL: Program Synthesis for Higher Order Logic Locking," in *International Conference on Tools and Algorithms for the Construction and Analysis of Systems* (TACAS 2022), Munich, Germany, April 2-7, 2022, pp. 1-16.
[doi: https://doi.org/10.1007/978-3-030-99524-9_1][arXiv: https://arxiv.org/abs/2201.10531]

IC.50. L. Collini, R. Karri, C. Pilato. "A Composable Design Space Exploration Framework to Optimize Behavioral Locking," in *Proceedings of IEEE Design, Automation & Test in Europe Conference* (DATE 2022), Antwerp, Belgium, March 14-23, 2022, pp. 1-6.
[doi https://doi.org/10.23919/DATE54114.2022.9774602]

IC.49. J. Bhandari, A. K. Thalakkattu Moosa, B. Tan, C. Pilato, G. Gore, X. Tang, S. Temple, P.-E. Gaillardon, R. Karri. "Exploring eFPGA-based Redaction for IP Protection," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design* (ICCAD 2021), *Virtual Conference*, November 1-5, 2021.
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WS.7. F. Cancare, C. Pilato, A. Cazzaniga, D. Sciuto, M.D. Santambrogio. "D-RECS: A Complete Methodology to Implement Self Dynamic Reconfigurable FPGA-Based Systems," in *Proceedings of 8th International Workshop on Reconfigurable Communication-centric Systems-on-Chip* (ReCoSoC 2013), Darmstadt, Germany, July, 10-12, 2013, pp. 1–7.
[doi: http://dx.doi.org/10.1109/ReCoSoC.2013.6581550]

WS.6. R. Cattaneo, X. Niu, C. Pilato, T. Becker, W. Luk, M.D. Santambrogio. "A Framework for Effective Exploitation of Partial Reconfiguration in Dataflow Computing," in *Proceedings of 8th International Workshop on Reconfigurable Communication-centric Systems-on-Chip* (ReCoSoC 2013), Darmstadt, Germany, July, 10-12, 2013, pp. 1–8.
[doi: http://dx.doi.org/10.1109/ReCoSoC.2013.6581535]

WS.5. G. Durelli, A. A. Nacci, R. Cattaneo, C. Pilato, D. Sciuto, M.D. Santambrogio. "A Flexible and Reconfigurable Interconnection Structure for FPGA Dataflow Applications," in *Proceedings of 20th Reconfigurable Architectures Workshop* (RAW 2013), Boston, MA, USA, May 20-21, 2013, pp. 1–8.
[doi: http://doi.ieeecomputersociety.org/10.1109/IPDPSW.2013.127]

WS.4. M.D. Santambrogio, D. Pnevmatikatos, K. Papadimitriou, C. Pilato, G. Gaydadjiev, D. Stroobandt, T. Davidson, T. Becker, T. Todman, W. Luk, A. Bonetto, A. Cazzaniga, G. Durelli, D. Sciuto. "Smart Technologies for Effective Reconfiguration: The FASTER approach," in *Proceedings of 7th International Workshop on Reconfigurable Communication-centric Systems-on-Chip* (ReCoSoC 2012), York, UK, July, 9-11, 2012, pp. 1–7.
[doi: http://dx.doi.org/10.1109/ReCoSoC.2012.6322881]

WS.3. G. Durelli, A. Cazzaniga, C. Pilato, M.D. Santambrogio, D. Sciuto. "Automatic Run-Time Manager Generation for Reconfigurable MPSoC Architectures," in *Proceedings of 7th International Workshop on Reconfigurable Communication-centric Systems-on-Chip* (ReCoSoC 2012), York, UK, July, 9-11, 2012, pp. 1–8.
[doi: http://dx.doi.org/10.1109/ReCoSoC.2012.6322883]

WS.2. C. Pilato, F. Ferrandi, D. Pandini. "Evaluating Static CMOS Complex Cells in Technology Mapping," in *Workshop on Exploiting Regularity in the Design of IPs, Architectures and Platforms* (ERDIAP 2011), Como, Italy, February 23, 2011, pp. 222-229.
[url: http://www.vde-verlag.de/proceedings-en/563333031.html]

WS.1. M. Elhoj, A. Reis, R. Ribas, F. Ferrandi, C. Pilato, F. Moll, M. Miranda, P. Dobrovolny, N. Woolaway, A. Grasset, P. Bonnot, G. Desoli, D. Pandini. "SYNAPTIC Project: Regularity Applied to Enhance Manufacturability and Yield at Several Abstraction Levels," in *Workshop on Exploiting Regularity in the Design of IPs, Architectures and Platforms* (ERDIAP 2011), Como, Italy, February 23, 2011, pp. 189-192 *(invited paper)*.
[url: http://www.vde-verlag.de/proceedings-en/563333026.html]

Workshop Publications with Informal Proceedings

WI.9. S. Soldavini, C. Pilato. "Compiler Infrastructure for Specializing Domain-Specific Memory Templates," in *Proceedings of the 1st Workshop on Languages, Tools, and Techniques for Accelerator Design* (LATTE) (held in conjunction with ASPLOS 2021), Virtual Event, April 15, 2021.
[arXiv: http://arxiv.org/abs/2104.01448]

WI.8. C. Pilato, F. Regazzoni. "High-Level Synthesis of Security Properties via Software-Level Abstractions," in *Proceedings of the 1st Workshop on Languages, Tools, and Techniques for Accelerator Design* (LATTE) (held in conjunction with ASPLOS 2021), Virtual Event, April 15, 2021.
[arXiv: http://arxiv.org/abs/2104.01446]

WI.7. C. Pilato, L.P. Carloni, F. Regazzoni. "Automatic generation of encrypted local memories for IoT devices," in *Proceedings of VLSI for IoT Workshop* (VLSI-IoT) (held in conjunction with DATE 2017), Lausanne, Switzerland, March 30, 2017. *(poster presentation)*

WI.6. P. Mantovani, E.G. Cota, S. Kim, K. Tien, J. Chan, G. Di Guglielmo, C. Pilato, M.A. Kim, M. Seok, K. Shepard, L.P. Carloni. "Benchmarking Methodology for Embedded Scalable Platforms," in *Proceedings of Workshop on Suite of Embedded Applications and Kernels* (SEAK 2014) (held in conjunction with DAC 2014), San Francisco, CA, USA, June 1, 2014. *(poster presentation)*.

WI.5. A.A. Nacci, C. Pilato, M.D. Santambrogio, D. Sciuto. "Designing Self-Adaptive Smart Spaces for Energy Saving," in *Proceedings of 2nd Workshop on Self-Awareness in Reconfigurable Computing Systems* (SRCS 2013), Porto, Portugal, September, 5, 2013, pp. 1–4.

WI.4. C. Pilato, R. Cattaneo, G. Durelli, A. Nacci, M.D. Santambrogio, D. Sciuto. "A2B: a Framework for the Fast Prototyping of Reconfigurable Systems," in *Proceedings of 7th HiPEAC Workshop on Reconfigurable Computing* (WRC 2013), Berlin, Germany, January, 21, 2013, pp. 1–10.

WI.3. C. Pilato, F. Ferrandi. "Improving Design Regularity by Targeting Custom Standard-Cell Libraries," in *Workshop on "Variability modelling and mitigation techniques in current and future technologies"* (VAMM 2012) (held during DATE 2012), Dresden, Germany, March 2012, *(poster presentation)*.

WI.2. F. Ferrandi, M. Lattuada, C. Pilato, D. Sciuto. "Performance Estimation for Mapping and Scheduling Parallel Applications on Heterogeneous Multi-Processor Systems," in *Workshop on "The European landscape of reconfigurable computing: Lessons learned, new perspectives and innovations"* (held during DATE 2010), Dresden, Germany, March 2010, *(poster presentation)*.

WI.1. C. Pilato, F. Ferrandi, P.L. Lanzi G. Palermo, A. Tumeo, D. Sciuto. "Bambu: a High Level Synthesis Framework with Evolutionary Design Space Exploration," in *Workshop on "The New Wave of the High-Level Synthesis"* (held during DATE 2008), Munich, Germany, March 2008, *(poster presentation)*.

Teaching Experience

Doctoral level

- **Lecturer**, "Advanced Topics in Hardware Security" - PhD in Information Technology (Politecnico di Milano) - 2022-2023.
- **Lecturer**, "Advances in System-on-Chip Design" - PhD in Information Technology (Politecnico di Milano) - 2019-2020.

Graduate level

- **Lecturer**, "Advanced Computer Architectures" - Computer Engineering (Politecnico di Milano) - 2023∼2024.
- **Lecturer**, "Design of Hardware Accelerators" - Computer Engineering (Politecnico di Milano) - 2021∼2023.
- **Lecturer**, "Computer Architecture and Operating Systems" - Geoinformatics Engineering (Politecnico di Milano) - 2021∼2023.
- **Lecturer**, "Digital System Design Methodologies 2" - Computer Engineering (Politecnico di Milano) - 2020-2021.
- Teaching assistant, "Digital System Design Methodologies 2" - Computer Engineering (Politecnico di Milano) - 2018∼2020.
- Teaching collaborator, "COMS E6998: Topics in Computer Science: Embedded Scalable Platforms" - Computer Science (Columbia University) - Spring 2015, Spring 2016.
- Teaching assistant, "Progettazione Hardware" - Computer Engineering (Politecnico di Milano) - 2010-2011, 2012-2013.
- Teaching assistant, "Metodologie di Progetto Hardware" - Computer Engineering (Politecnico di Milano) - 2008-2009.

Undergraduate level

- **Lecturer**, "Fondamenti di Informatica per il Web Design" - Communication Design (Politecnico di Milano) - 2021∼2023.
- **Lecturer**, "Elementi di Informatica e Reti di Calcolatori" - Communication Design (Politecnico di Milano) - 2018∼2021.
- **Lecturer**, "Informatica" - Space Engineering (Politecnico di Milano) - 2018∼2020.
- Teaching assistant, "Architetture dei Calcolatori e Sistemi Operativi" - Computer Engineering (Politecnico di Milano) - 2019-2020.
- Teaching assistant, "Reti Logiche" - Online Degree on Computer Engineering (Politecnico di Milano) - 2018-2019.
- Teaching assistant, "Reti Logiche" - Computer Engineering (Politecnico di Milano) - 2007∼2012, 2017-2018.
- Teaching assistant, "Architetture dei Calcolatori e Sistemi Operativi" - Telecommunications Engineering (Politecnico di Milano) - 2009∼2012.

- Lab supervisor, "Informatica A" - Mathematical Engineering (Politecnico di Milano) - 2011-2012.
- Teaching assistant, "Informatica 2" - Telecommunications Engineering (Politecnico di Milano) - 2008-2009.
- Lab tutor, "Informatica 2" - Telecommunications Engineering (Politecnico di Milano) - 2007-2008.

PhD Students' Advisor

- *Mattia Tibaldi*, "Adaptive Heterogeneous Computing for Reducing Carbon Emissions of FPGA Data Centers" (2021-*ongoing*)
- *Stephanie Soldavini*, "Design Methods for Simplifying the Creation of Domain-Specific Memory Architectures" (2020-*ongoing*)

PhD Students' Opponent

- *Zain Ul Abideen*, "Leveraging FPGA Reconfigurability as an Obfuscation Asset," advisor: Samuel Pagliarini (Tallinn University of Technology), 2024
- *Mohammad Amir Mansoori*, "FPGA Acceleration of Domain-specific Kernels via High-Level Synthesis," advisor: Mario Casu (Politecnico di Torino), 2022
- *Anh Hoang Ngoc Nguyen*, "Amoeba-Inspired SAT Solver on IoT Edge Devices," advisor: Yuko Hara-Azumi (Tokyo Institute of Technology), 2021
- *Hannah Badier*, "Transient Obfuscation for HLS Security," advisor: Philippe Coussy (Ecole Nationale Supérieure de Techniques Avancées (ENSTA) Bretagne), 2021

MSc Students' Advisor

- *Marco Colombi*, "Flexible logic locking obfuscation for sequential circuits through synchronous configurable blocks", 2023.
- *Nicolò Campanini* and *Salvatore Torsello*, "Design and optimization of an FPGA-based system for real-time human stress level assessment", 2023.
- *Leonel Gouveia Ergin*, "On the Design of Multi-directional Systolic Arrays for Band and Generic Matrix-Matrix Multiplications", 2022.
- *Luca Collini*, "Composable Heuristics for RTL Logic Locking Optimization based on System Dependence Analysis", (part of this thesis has been published in [IC.50]), 2021.
- *Davide Toschi* and *Leonardo Terlizzi*, "Leonardo: A New Ultra-Low Power Central Processing Unit for Energy Harvesting", 2021.
- *Marco Speziali*, "ISAbella: An Instruction Set Architecture for Ultra Low-Power Processor Design", 2021.

Visiting Students' Supervision

- Raul Murillo, Complutense University of Madrid, Spain (2021)
- Anh Hoang Ngoc Nguyen, Tokyo Insititute of Technology, Japan (2020 - *virtual internship*)
- Hannah Badier, ENSTA Bretagne - Lab-STICC, France (2019)

Students' Supervision

- *Donald Gazidedjia*, "HW-SW architectures for security and data protection at the edge", advisor: S. Zanero, 2021.
- *Mattia Tibaldi*, "A System-on-Chip Platform for the Protection of On-Chip Communications", advisor: F. Ferrandi, (part of this thesis has been published in [JR.16]), 2021.
- *Bernardita Alejandra Stitic Leiva* (Politecnico di Torino), "A multiclass neural network model for contaminant detection in hazelnut-cocoa spread jars", advisor: M. Casu (in collaboration with Politecnico di Torino and Columbia University - student from Alta Scuola Politecnica), 2020.
- *Antonio Verlotta*, "Designing a Quantum Error Correction System on FPGA", advisor: D. Sciuto (in collaboration with the Quantum Information Science Theory Group at the National Institute of Informatics, Tokyo, Japan), 2014.
- *Matteo Mastinu*, "Design Flow to Support Dynamic Partial Reconfiguration on Maxeler Architectures", advisor: M.D. Santambrogio (in collaboration with Maxeler Technologies, London, UK, part of this thesis has been published in [IC.27] and won the "2012 HiPEAC Technology Transfer Award"), 2012.
- *Gianluca Durelli*, "A^2B: Application to Bitstream. Flusso semi automatico per lo sviluppo di MPSoC riconfigurabili", advisor: D. Sciuto, (part of this thesis has been in published in [WS.3][IC.18][IC.19]), 2012.

- *Stefano Manni*, "A Methodology for Improving the Library-Free Logic Synthesis of Integrated Circuits", advisor: F. Ferrandi, 2012.
- *Vito Giovanni Castellana* and *Silvia Lovergine*, "A Design Methodology for Efficient HLS Controllers", advisor: F. Ferrandi, (part of this thesis has been published in [IC.16]), 2010.
- *Luca Sisler*, "Metodologie di progetto per circuiti regolari", advisor: F. Ferrandi, 2010.
- *Andrea Conti*, 'Technology Mapping for Dynamic Cell Generation based on Canonical Boolean Matching", advisor: F. Ferrandi, 2009.
- *Francesca Malcotti*, "High-Level Synthesis optimization combining speculative execution and SSA-based liveness analysis", advisor: F. Ferrandi, 2008.
- *Gerardo Gallucci*, "Regularity-aware synthesis and regularity extraction from circuit RTL and structural logical representation", advisor: F. Ferrandi (in collaboration with STMicroelectronics, Agrate, MI, Italy), 2008.

In addition, Christian Pilato supervised the activity of around 20 M.Sc. and 3 Ph.D. students at Politecnico di Milano, and 2 students at Columbia University.

Academic Service

- Responsible for the Short-Mobility Program (Erasmus+) 2022 – *present*
  Computer Science, Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano
- Member of the Internationalization Group 2020 – *present*
  Computer Science, Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano

Professional Service

Membership Services

- *ACM Europe Research Visibility* working group (member and secretary) *2021 – present*

Conference and Workshop Organization

- PhD Forum Chair (DATE Executive Committee (DEC) Member) for the IEEE/ACM International Conference on Design, Automation, and Test in Europe (DATE 2025)
- **General Chair** for the 42nd IEEE International Conference on Computer Design (ICCD 2024)
- Track Chair ("2.1 - High-Level, Behavioral, and Logic Synthesis and Optimization") for the IEEE/ACM International Conference on Computer-Aided Design (ICCAD 2024)
- Track Chair ("Track 5 - Architectures, Compilers, System-level Design") for the IEEE/ACM International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES 2024)
- **Program Chair** for the International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (IC-SAMOS 2024)
- PhD Forum Chair (DATE Executive Committee (DEC) Member) for the IEEE/ACM International Conference on Design, Automation, and Test in Europe (DATE 2024)
- Track Chair ("2.1 - High-Level, Behavioral, and Logic Synthesis and Optimization") for the IEEE/ACM International Conference on Computer-Aided Design (ICCAD 2023)
- **Program Chair** for the 41st IEEE International Conference on Computer Design (ICCD 2023)
- Organizing Co-Chair for the 5th Scientific School on "Designing Cyber-Physical Systems – From concepts to implementation", Alghero, Italy, September 8-22, 2023
- Track Chair ("Track 5 - Architectures, Compilers, System-level Design") for the IEEE/ACM International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES 2023)
- Journal-Track Chair for the 33rd IEEE International Conference on Field-Programmable Logic and Applications (FPL 2023)
- **Program Chair** for the International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (IC-SAMOS 2023)
- **Vice General Chair** for the 31st IEEE International Symposium On Field-Programmable Custom Computing Machines (FCCM 2023)
- Topic Chair ("D2 - System-Level Design Methodologies and High-Level Synthesis") for the IEEE/ACM International

Conference on Design, Automation, and Test in Europe (DATE 2023)
- PhD Forum Chair (DATE Executive Committee (DEC) Member) for the IEEE/ACM International Conference on Design, Automation, and Test in Europe (DATE 2023)
- Organizer of the Special Session on "Hardware Security Through Reconfigurability: Attacks, Defenses, and Challenges" at the IEEE/ACM International Conference on Computer-Aided Design (ICCAD 2022)
- **Program Chair** for the 40th IEEE International Conference on Computer Design (ICCD 2022)
- Organizing Chair for the 3rd Workshop on "DevOps Support for Cloud FPGA platforms", held in conjunction with the IEEE International Conference on Field-Programmable Logic and Applications (FPL 2022), Belfast, United Kingdom, September 1, 2022
- Track Co-Chair ("2.1 - High-Level, Behavioral, and Logic Synthesis and Optimization") for the IEEE/ACM International Conference on Computer-Aided Design (ICCAD 2022)
- Track Chair ("Track 5 - Architectures, Compilers, System-level Design") for the IEEE/ACM International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES 2022)
- Organizer of the Special Session on "Security during system level design: Small step or giant leap?" at the IEEE/ACM Design Automation Conference (DAC 2022)
- Track Chair ("EDA4 - RTL/Logic Level and High-level Synthesis") for the IEEE/ACM Design Automation Conference (DAC 2022)
- Organizing Chair for the 1st PhD School on "Extreme-scale big data analytics and scientific computing on heterogeneous platforms", Lake Como, Italy, Summer 2022
- Organizing Co-Chair for the Workshop on "Data-driven applications for industrial and societal challenges: Problems, methods, and computing platforms," held in conjunction with the IEEE/ACM International Conference on Design, Automation & Test in Europe (DATE 2022)
- Organizing Co-Chair for the 4th Scientific School on "Designing Cyber-Physical Systems – From concepts to implementation", Pula, Italy, September 19-23, 2022
- Topic Co-Chair ("D2 - System-Level Design Methodologies and High-Level Synthesis") for the IEEE/ACM International Conference on Design, Automation, and Test in Europe (DATE 2022)
- Organizing Chair for the Workshop "Design and Programming High-performance, distributed, reconfigurable and heterogeneous platforms for extreme-scale analytics", held in conjunction with European Network on High-performance Embedded Architecture and Compilation Conference (HIPEAC 2022), January 2022
- Organizer of the Special Session "EVEREST: High-Performance, Distributed, Reconfigurable and Heterogeneous Platforms for Extreme-Scale Data Analytics" at the European Big Data Value Forum (EBDVF 2021)
- Topic Co-Chair ("D2 - System-Level Design Methodologies and High-Level Synthesis") for the IEEE/ACM International Conference on Design, Automation, and Test in Europe (DATE 2021)
- Organizing Co-Chair for the 3rd Scientific School on "Designing Cyber-Physical Systems – From concepts to implementation", Porto Conte Ricerche, Italy, September 23-27, 2019
- Organizing Co-Chair for the 2nd Scientific School on "Designing Cyber-Physical Systems – From concepts to implementation", Alghero, Italy, September 17-21, 2018
- Organizing Co-Chair for the 1st Scientific School on "Designing Cyber-Physical Systems – From concepts to implementation", Porto Conte Ricerche, Italy, September 25-30, 2017
- **Program Chair** for the 12th IEEE/IFIP International Conf. on Embedded and Ubiquitous Computing (EUC 2014)
- Organizing Chair for the Workshop on "ReconfigurAble Computing for Embedded Systems" (RACES 2014), held in conjunction with the IEEE/ACM Design Automation Conference (DAC 2014)
- Program Vice-Chair and Track Chair ("Embedded System Architectures") for the 11th IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC 2013)
- Organizing Co-Chair for the Workshop on "Variability modelling and mitigation techniques in current and future technologies" (VAMM 2012), held in conjunction with the IEEE/ACM International Conference on Design, Automation & Test in Europe (DATE 2012)

Conference and Workshop Service
- Tutorial Chair for the 2024 Embedded Systems Week (ESWEEK 2024)
- Publicity Chair for the 31st Reconfigurable Architectures Workshop (RAW 2024)

- Publicity Chair for the IEEE Forum on specification & Design Languages (FDL 2023)
- Publicity Chair for the 33rd IEEE International Conf. on Field-Programmable Logic and Applications (FPL 2023)
- Tutorial Committee Member for the International Conference for High Performance Computing, Networking, Storage, and Analysis (SC 2023)
- Jury Member for the ACM Student Research Competition at the 41st IEEE/ACM International Conference on Computer-Aided Design (ICCAD 2022)
- Publicity Chair for the 33rd IEEE International Conf. on Application-Specific Systems, Architectures, and Processors (ASAP 2022)
- Tutorial Committee Member for the International Conference for High Performance Computing, Networking, Storage, and Analysis (SC 2022)
- Jury Member for the ACM Student Research Competition at the 40th IEEE/ACM International Conference on Computer-Aided Design (ICCAD 2021)
- Member of the Best Paper Award Committee for the 31st IEEE International Conf. on Field-Programmable Logic and Applications (FPL 2021)
- Publicity Chair for the 31st IEEE International Conf. on Field-Programmable Logic and Applications (FPL 2021)
- Publicity Chair for the 28th IEEE Reconfigurable Architectures Workshop (RAW 2021)
- Publicity Chair for the 30th IEEE International Conf. on Field-Programmable Logic and Applications (FPL 2020)
- Local Arrangement Chair for the ACM/IEEE International Symposium on Networks-on-Chip (NOCS 2019)
- Special Session and Tutorial Chair for the 37th IEEE International Conference on Computer Design (ICCD 2019)
- Publicity Chair for the ACM International Conference on Computing Frontiers (CF 2019)
- Tutorial Chair for the 36th IEEE International Conference on Computer Design (ICCD 2018)
- Special Session and Tutorial Chair for the 35th IEEE International Conference on Computer Design (ICCD 2017)
- Special Session and Tutorial Chair for the 34th IEEE International Conference on Computer Design (ICCD 2016)
- Special Session and Tutorial Chair for the 33rd IEEE International Conference on Computer Design (ICCD 2015)
- Publicity Chair for the 10th IEEE NASA/ESA Conference on Adaptive Hardware and Systems (AHS 2015)
- Publicity Chair of the 9th IEEE International Conference on Networking, Architecture, and Storage (NAS 2014)

Editorial Board

- **Associate Editor**, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (2024 – *present*)
- **Associate Editor**, *Foundations and Trends in Electronic Design Automation* (2022 – *present*)
- Topical Advisory Panel Member, *MDPI Electronics* (2022 – *present*)
- **Associate Editor**, *IEEE Access* (2020 – *present*)
- Guest Editor, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, "High-Level Synthesis for FPGA: Next-Generation Technologies and Applications" [http://dx.doi.org/10.1145/3519279] (2021)
- Guest Editor, *MDPI Electronics*, "Advances in System-on-Chip Design" (2021)
- Guest Editor, *ACM Transactions on Embedded Computing (TECS)*, "Special issue on Innovative design methods for smart embedded systems" [http://dx.doi.org/10.1145/2885505] (2016)

Technical Program Committee Work

Conferences

- IEEE/ACM International Conference on Computer-Aided Design (ICCAD), (2020, 2021, 2022, 2023, 2024)
- Baltic Electronics Conference (BEC), (2024)
- IEEE/ACM International Conference on Compilers, Architecture, and Synthesis of Embedded Systems (CASES), (2016, 2017, 2018, 2019, 2020, 2021, 2022, 2023, 2024)
- IEEE International Conference on Field-Programmable Logic and Applications (FPL), (2015, 2016, 2017, 2018, 2019, 2020, 2021, 2022, 2024)
- IEEE Forum on specification & Design Languages (FDL), (2024)
- IEEE International Symposium On Field-Programmable Custom Computing Machines (FCCM), (2024)
- Conference on Design and Architectures for Signal and Image Processing (DASIP), (2017, 2018, 2019, 2021, 2022, 2023, 2024)
- Euromicro Conference on Digital System Design (DSD), (2023)

- IEEE/IFIP Symposium on Integrated Circuits and Systems Design (SBCCI), (2018, 2019, 2020, 2021, 2022, 2023)
- IEEE/ACM International Conference on Design, Automation, and Test in Europe (DATE), (2015, 2016, 2018, 2019, 2020, 2021, 2022, 2023)
- IEEE Computer Society Annual Symposium on VLSI (ISVLSI), (2020, 2021, 2022, 2023)
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), (2023)
- IEEE/ACM Design Automation Conference (DAC), (2020, 2021, 2022)
- IEEE International Conference on Field-Programmable Technology (FPT), (2022)
- IEEE International Conference on Computer Design (ICCD), (2019, 2020)
- IEEE NASA/ESA Conference on Adaptive Hardware and Systems (AHS), (2015, 2016, 2017, 2018, 2019)
- IEEE Southern Programmable Logic Conference (SPL), (2012, 2013, 2014, 2019)
- IEEE International Conference on ReConFigurable Computing and FPGAs (ReConFig), (2012, 2013, 2014, 2015, 2018)
- Symposium on Parallel Computing with FPGAs (ParaFPGA), (2017)
- ACM International Conference on Computing Frontiers (CF), (2016, 2017)
- International Symposium on Applied Reconfigurable Computing (ARC), (2014, 2015, 2016, 2017)
- IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC), (2012, 2013, 2014, 2015)

Workshops

- Workshop on Safety and Security in Heterogeneous Open System-on-Chip Platforms (SSH-SoC), (2024)
- IEEE International Reconfigurable Architectures Workshop (RAW), (2013, 2014, 2015, 2021, 2024)
- International Workshop on Safety and Security in Heterogeneous Open System-on-Chip Platforms (SSH-SoC), (2023)
- International Workshop on Research Open Automatic Design for Neural Networks (DAC-ROAD4NN), (2022)
- IEEE/ACM Design Automation Conference Late Breaking Results (DAC-LBR), (2020, 2022)
- HiPEAC Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO), (2014, 2015, 2016, 2017, 2018, 2019, 2020, 2021)
- International Workshop on Top Picks in Hardware and Embedded Security, (2018)
- International Workshop on Big Data Analytics (BigDAW), (2017)
- International Workshop on Reliability, Security and Quality (RESCUE), (2017)
- IEEE Workshop on Virtual Prototyping of Parallel and Embedded Systems (ViPES), (2015, 2016)
- HiPEAC Workshop on Reconfigurable Computing (WRC), (2014, 2015, 2016)
- Workshop on Variability modeling and mitigation techniques in current and future technologies (VAMM), (2012)
- Workshop on Exploiting Regularity in the Design of IPs, Architectures and Platforms (ERDIAP), (2011)

Reviewer Role for Conferences and Journals

- IEEE Access
- ACM Transactions on Embedded Computing (TECS)
- ACM Transactions on Architecture and Code Optimization (TACO)
- ACM Transactions on Reconfigurable Technology Systems (TRETS)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- ACM Computing Surveys (CSUR)
- IEEE Transactions on Emerging Topics in Computing
- IEEE Design & Test (D&T)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Evolutionary Computation (TEC)
- IEEE Transactions on Computers (TC)
- IEEE Embedded Systems Letters (ESL)
- IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)
- Elsevier International Journal on Systems Architecture (JSA)
- International Journal of Signal Processing Systems (JSPS)
- International Journal on Microprocessors and Microsystems (MICPRO)
- International Journal of High Performance Systems Architecture (IJHPSA)
- International Journal on Design Automation for Embedded Systems (DAES)

- IEEE/ACM Design Automation Conference (DAC)
- IEEE/ACM International Conference on Design, Automation, and Test in Europe (DATE)
- IEEE/ACM International Symposium on Computer Architecture (ISCA)
- IEEE International Conf. on Hardware/Software Codesign and System Synthesis (CODES+ISSS)
- IEEE International Parallel & Distributed Processing Symposium (IPDPS)
- IEEE/ACM International Symposium on Networks-on-Chip (NOCS)
- IEEE/ACM International Conference on Embedded Software (EMSOFT)
- IEEE International Conference on Field Programmable Logic and Applications (FPL)
- IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)
- IEEE International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS)
- IEEE International Symposium on Circuits and Systems (ISCAS)

Memberships

- **DISCOVER-US Member** *2024 – present*
- **ACM Senior Member** *2020 – present*
- **IEEE Senior Member** *2019 – present*
- **HiPEAC Member** *2018 – present*
- ACM Member *2015 – 2020*
- IEEE Member *2011 – 2019*
- HiPEAC Affiliated Member *2008 – 2018*
- IEEE Student Member *2007 – 2011*

Presentations

Keynote Presentations at Conferences and Workshops

- "Data and IP protection in heterogeneous system-on-chip architectures" at the HiPEAC Workshop on Rapido Simulation and Performance Evaluation (RAPIDO 2021), *Virtual Event*, January 20, 2021
- "High-Level Synthesis: where we are and we are going" at the IEEE International Conference on Field-Programmable Technology (FPT 2017), Melbourne, Australia, December 13, 2017.
- "Bridging the Gap between Software and Hardware Designers" at the symposium on Parallel Computing with FPGAs (ParaFPGA 2017), held in conjunction with ParCo 2017, Bologna, Italy, September 12, 2017

Invited Talks at Conferences, Workshops, and Summer Schools

- "Enhancing hardware security and trust with high-level design methods", at the Special Session on Hardware Security at the International Workshop on Logic Synthesis (IWLS), Lausanne, Switzerland, June 6, 2024
- "Bridging the gaps among application, hardware, and system designers: The EVEREST experience", at the "Big Data technologies and extreme-scale analytics" Projects Workshop (organized by BDVA/EC), *Virtual*, September 27, 2022
- "Designing memory architectures with high-level synthesis: What could possibly go wrong?" at the 1st Workshop Formal Methods in High-Level Synthesis (FLASHLIGHT), held as part of the 30th IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM 2022), New York, NY, USA, May 18, 2021
- "Climbing EVEREST: A design environment for extreme-scale big data analytics on heterogeneous platforms" at the Workshop on DevOps Support for Cloud FPGA platforms (cFDevOps 2021), held in conjunction with the IEEE International Conference on Field-programmable Logic and Applications (FPL 2021), *Virtual Event*, August 30, 2021
- "Accelerator Memory Design for Heterogeneous System-on-Chip Architectures" at the Memory Architecture and Organization Workshop (MeAOW 2014), held in conjunction with the Embedded System Week (ESWEEK 2014), New Delhi, India, October 16, 2014
- "Emerging challenges and trends in hardware acceleration for adaptive systems" at the Workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHA'N'GE 2014), held in conjunction with the 51st Design Automation Conference (DAC 2014), San Francisco, CA, USA, June 1, 2014
- "A2B: a Framework for the Fast Prototyping of Reconfigurable Systems" at the Workshop on Reconfigurable Computing (WRC 2013), Berlin, Germany, January 21, 2013

- "On the Automatic Creation of Custom Standard-Cell Libraries" at the Workshop on Methods and tools to cope with the design challenges in the next generations of technologies, Milano, Italy, May 16, 2012
- "A Design Exploration Framework for Mapping and Scheduling onto Heterogeneous MPSoCs" at the 3rd Workshop on Mapping Applications to MPSoCs, St. Goar, Germany, June 29-30, 2010

Conference Tutorials

- "Embedded FPGAs (eFPGA) and Applications to IP Protection via eFPGA Redaction" at the IEEE/ACM Design, Automation and Test in Europe Conference (DATE 2023), Antwerp, Belgium, April 17-19, 2022
- "Electronic system-level design for hardware IP protection" at the 35th SBC/SBMicro/IEEE/ACM Symposium on Integrated Circuits and Systems Design (SBCCI 2022), Virtual Conference, August 22, 2022 (**invited**)
- "Bambu: An open-source framework for research in high-level synthesis" at the IEEE International Conference on Field-Programmable Technology (FPT 2017), Melbourne, Australia, December 14, 2017 (**invited**)
- "Designing Multi-Bank Memories for Heterogeneous Architectures" at the ACM/IEEE Embedded Systems Week (ESWEEK 2017), Seoul, South Korea, October 15, 2017
- "Bambu: An open-source framework for research in high-level synthesis" at the IEEE International Conference on Field-Programmable Logic and Applications (FPL 2017), Ghent, Belgium, September 7, 2017

Academic Seminars

- "Enhancing hardware security and trust with high-level design methods", at Tallinn University of Technology, Tallin, Estonia, January 15, 2024
- "Modern trends in accelerator design with high-level synthesis" at Swiss Federal Institute of Technology (ETH), Zurich, Switzerland, November 28, 2022
- "Generating HPC memory architectures with HLS: The two sides of the medal" at New York University, New York, NY, USA, May 18, 2022
- "High-level synthesis of HPC memory architectures" at the Politecnico di Torino, Torino, Italy, April 27, 2022
- "Automatic generation of hardware memory architectures for HPC" at Complutense University of Madrid, Madrid, Spain, April 21, 2022
- "Electronic system-level design for data and IP protection" at Technische Universitat Dresden, Dresden, Germany, November 23, 2021
- "Protecting data and intellectual property in accelerator-rich architectures with high-level methods" at Complutense University of Madrid, Madrid, Spain, June 16, 2021
- "Hardware security and high-level synthesis: the good, the bad and the ugly" at Columbia University, New York, NY, USA, November 9, 2018
- "Optimizing private local memories in heterogeneous architectures" at University of California Irvine (UCI), Irvine, CA, USA, June 14, 2017
- "Designing and Optimizing Hardware Accelerators with Private Local Memories" at Swiss Federal Institute of Technology (ETH), Zurich, Switzerland, May 24, 2017
- "TaintHLS: Enabling Dynamic Information Flow Tracking in Hardware Accelerators" at New York University (NYU), New York, NY, USA, November 2, 2016
- "System-Level Memory Optimization for Heterogeneous System-on-Chip Architectures" at Università della Svizzera italiana (USI), Lugano, Switzerland, January 16, 2015
- "Design Challenges and Techniques for Heterogeneous Reconfigurable Systems" at École Polytechnique, Montréal, QC, Canada, September 26, 2013
- "On the Automatic Synthesis of Hardware Accelerators for Improving Embedded Systems" at Columbia University, New York, NY, USA, May 23, 2013
- "Accelerating research in reconfigurable computing: the FASTER approach" at Massachusetts Institute of Technology (MIT), Boston, MA, USA, May 22, 2013

Industrial Seminars

- "A Guide into the Galaxy of High-Level Synthesis" at Google X, *Virtual*, September 16, 2022
- "PandA-Bambu: A free software framework for the High-Level Synthesis of Complex Applications" at European Space Research and Technology Centre (ESA-ESTEC), Noordwijk, The Netherlands, April 12, 2012

- "Field Programmable Gate Array (FPGA): design and testability" at Alenia AerMacchi, Venegono Inferiore (VA), Italy, February 3, 2008

References

- Donatella Sciuto, Professor and Rector
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