Michele Chiabrera

SUMMARY

Michele Chiabrera is INVENTVM Semiconductor co-founder and CEO, with more than 24 years of leadership in the semiconductor industry. He held senior management/director of R&D positions in STM, Marvell Semiconductor and Silicon Mitus Italy, were he also served as BoD member. His expertise spans over multiple market segments ranging from networking to mobile, audio and power management through a wide skillset covering technical marketing, digital, DSP, SW and system engineering.

He has a proven track record in creating breakthrough product lines and new market segments, as well as founding and developing successful design centers (Silicon Mitus Italy, Marvell Italy). Michele is a technology enthusiast and strives to leave the earth a better place. His core strength can be summarized with a simple statement: "Making it happen" in everything he approaches. He holds a MSEE degree with honors at the University of Genoa (1999) and teaches as a contract professor at the University of Genoa & University of Pavia.

PROFESSIONAL EXPERIENCE

INVENTVM Semiconductor, Pavia, ITALY 2/2021 - present

CEO & Co-Founder ***2/2021 – present***

- Founded INVENTVM Semiconductor as a management buyout of Silicon Mitus Italy
- Providing overall company guidance, with direct responsibility of business development and strategy

SILICON MITUS, Pavia, ITALY 6/2017- 1/2021

Senior Director of Engineering ***6/2017 – 1/2021***

- Managing Silicon Mitus Italy R&D operations, consisting of a group of 40 engineers focused on power management and audio codec product lines for mobile/consumer
- Defining the site product/ IP roadmaps and contributing to the overall company strategy interacting directly with the CEO/CFO
- I lead all PMIC, charger and audio codec product, IP architecture and system definition efforts interacting directly with internal and external customers and design teams
- Specific system/IP expertise: Switching/linear chargers/regulators, high voltage/buck boost/direct charging, USB TYPE-C & PD, Camera flash, fuel gauge, wireless charging (Qi/PMA/A4WP) design/certification, boosted Class-D, speaker protection, ultra HiFi audio DAC/ADC & DSP, mic/jack handling, RGB/LCD lighting, headset PA, RTC, XO

MARVELL SEMICONDUCTOR, Pavia, ITALY 3/2007-5/2017

Engineering director of PMIC and audio codec development 1/2015 – 5/2017

- Managing a group of up to 45 engineers in Marvell Italy with responsibility over Marvell's power management and audio codec product lines for mobile, consumer, automotive and IoT
- I Redefined BU product/ IP roadmaps, product definition and business plan with 3 years visibility after Marvell's exit from mobile segment, leading the group transition to a self-contained power management business unit with its own mission and P&L responsibility

Staff Manager of high-speed digital, PMIC and HW/Application group 3/2007 – 1/2015

- Managing a group of 30 designers, including the Marvell Italy digital team, in charge of developing the digital portions of Marvell audio codecs, PMICs and ADC based high speed SERDES systems as well as Marvell global AE PMIC HW and SW support
- I defined and setup the digital and mixed signal design flow used by Marvell Italy.
- I lead the development and digital/system level definition of a 56Gb/s ADC based Pam4 – 28Gb/s NRZ serdes with proven first-time silicon results.
- The lab silicon validation responsibility for PMIC and codec products lied within my team, streamlined through fully automated setups, as well as R&D lab activities on innovative charging, fuel gauging, power optimization and audio DSP algorithms.
- Hundreds of millions mobile phones and tablets on the market use Marvell PMICs, codecs and chargers developed by my team or myself as project leader.

ST MICROELECTRONICS, Ottawa, CANADA 1999-3/2007

Design Manager – High Speed digital IP 9/ 2006 – 3/2007

- During my professional career in ST Microelectronics, I have been working as a system and digital designer first, then project leader and design manager of a group developing the digital portion of telecommunications systems over copper and backplane channels, following the 802.3 standard development from 10Mbit/s Base-T devices to 10Gbit/s PHYs.

Project leader – ASIC development 2003 – 9/2006

Starfighter MultiGigaBaud (1.25 – 7.5 GBaud/s) transceiver design - 65nm

IEEE 802.3 1000Base-T transceiver design – 90 nm

IEEE 802.3 10/100Base-TX transceiver design – 90 nm

IEEE 802.3 1000Base-T gigabit transceiver design – .18um

Digital/system designer ***1999 – 2003***

IEEE 802.3 1000Base-T gigabit transceiver DSP and MAC design - .18um

ITU G.992.2 ADSL modem design & system .

VoIP-Powerline modem design & system

PROFESSIONAL DEVELOPMENT

- CAD tools expertise: most tools used in front end Synopsys/Cadence flows (Design Compiler, PrimeTime, Formality, ncsim, verilog-xl, VCS, DFT compiler, Specman, Genus/Innovus/Tempus), Verdi, Matlab, Verilog/VHDL HDL, e-code, C, C++.

- Professional training: VHDL, IP reuse, Design Sync, Smartbits Ethernet test equipment, Synopsys Primetime, Cadence Tensilica. Specman, ARM Cortex M3, UVM

EDUCATION

- Master degree (110/110 cum laude) in Electronic Engineering University of Genoa, Italy
- Professional Engineer Albo ingegneri, Italy
- High School diploma "Liceo classico A. D'Oria (58/60)" Genoa, Italy

CITIZENSHIP AND LANGUAGES

- Italian and Canadian citizen.
- Fluent English and Italian**,** basic Mandarin, Spanish and French.

PERSONAL INTERESTS

- Skiing, trekking, soccer, guitar playing and music.

PATENTS GRANTED AND PENDING

- "A method for transmission and recovery of a 4-lane 8B/10B encoded data path into 1-lane or 2-lane 8B/10B encoded data path", 2005
- "A method for Transmission and recovery of a 64B/66B encoded data stream across multiple Physical Medium Attachments", 2005
- "A method for encoding and decoding running disparity information over 64B/66B and 192B/200B coding systems", 2006
- "A method for recovering lane alignment on multi-lane 10GBase-R systems", 2006
- "A modular FIR architecture", 2006
- "Cable tester system", 2006
- "IP phone detection system", 2005
- "A method to recover lane alignment in 10GBase-X systems with lane skew greater than 85UI", 2006
- Technique to realize a temperature compensation for 26MHz clock generation in mobile application, 2015
- "adaptive control of capacitive load", 2022