Curriculum Vitae
Daniele Grosso



Short personal profile

I am a serious and motivated professional, self-driven and used to deliver against schedule and objectives, very good at mixing with people and settling into new environments.

Motivations

Working as a consultant allows me to face new challenges, pursue new opportunities and further develop my skills and competences. I have a solid technical background enriched by a very intense experience of management.

Current Position

Since 2015 I'm co-owner and managing director of Insyde SRLs company which provides services in the context of digital IC design, electronic and microelectronic product and system development. I also have a regular collaboration with the DITEN department of the University of Genoa where I'm an external professor and I teach in two courses of microelectronic.

Core Competence

I'm an experienced digital IC design engineer specialized in ASIC, SoC as well as FPGA design with a wide knowledge of all the aspects of the Front End Flow from architecture definition and specification writing to implementation, including RTL design (VHDL, verilog and system verilog) and verification (including UVM and coverage driven constraint random verification).

Working history

May 2015 –Today

Company	Insyde SRLs.
Company Business Model	Design Services
Job Title	Co –owner and managing director
Main Responsibilities	Company Legal representative
	Account manager
	Technical leadership and supervision
	Projects definition and coordination
	ASIC SoC and FPGA design & verification
	System and architectural design

Since May 2015 I have worked in the following projects (confidentiality on customer name applies).

- **Verification on 10BASE-T1S Multi-drop MAC/PHY chip** (01/2024 today) Verification Leader for the Digital part of the chip. Planning, Verification architecture, day to day team supervision, regression set up, coverage closure, gate level simulation, verification reports.

- **Pressure and Temperature Sensing system** (07/2023 – 01/2024): Contract with Infineon on an integrated temperature and pressure sensor IC with internal heating capabilities. My tasks and responsibilities included verifying the "heater". Discussed with the end customer the verification plan, developed the UVM components (passive agent, scoreboard, tests and coverage model), added to the top level testbench, and taken the IP to code and functional coverage closure.

- **Digital Camera Interface - Soc for mobile applications** (08/2019 – 06/2023): Contract with Infineon on a complex SoC for 3D imaging reconstruction. My tasks and responsibilities included building a UVM testbench for a CSI2 IP and contributing to all the aspects of the top level UVM testbench.

- **Audio Video Processing SoC:** (09/2018 – 07/2019): Contract with Adesto Technologies. This was to work on a complex SoC for audio and video processing. My tasks and responsibilities included design and verification activities with particular attention to the MIPI DSI 3rd party IP and top level functional verification.

- **USB3.1 Portfolio:** (09/2016 – 09/2018): Contract with a prime EDA and IP solution vendor. This was to develop a UVM verification environment for the existing and under development IPs in the customer portfolio.

- **Security Controller @ Infineon AG:** (02/2016 – 09/2016): Architectural and RTL design consultancy for Infineon AG (ChipCard) to develop the new generation product for security applications. Such product consists on a processor with advanced security features based on a customized commercial core.

- **USB3.0 IP Portfolio:** (06/2015 – 12/2015): Technical Leader on a UVM complex and configurable testbench used to demo all the existing IP in the customer portfolio. That includes USB2.0 and USB3.0 xHCI, SSDEV, DRD with OTG capabilities.

May 2009 –May 2015y

Company	Skyco di Grosso Daniele (Freelance Consultant).
Company Business Model	Consultancies
Job Title	Owner
Main Responsibilities	ASIC SoC and FPGA design & verification
	System and architectural design
	R&D Projects definition and coordination
	Didactic activities
	Project and working group management

I started to work as a freelance consultant in May 2009. The list of the projects I have worked on follows (confidentiality on customer name applies).

- **USB3.0 Controller**: (01/2015 – 05/2015): RTL Design and System Verilog verification of a USB3.0 xHCI controller.
- **MIPI MPHY @ INTEL IMC**: (01/2014 – 12/2014): Architectural and RTL Design and System Verilog verification of a MIPI MPHY core. System-Verilog modelling of Analog Front End circuitry.
- **MIPI Display Serial Interface**: (09/2013 –12/2013): MIPI DSI Host Controller IP
- **Multiprotocol Multispeed Network Adapter** (11/2012 – 08/2013): Testchip including a multiprotocol multispeed newtwork adatpter for the consumer electronic market
- **NVME controller** (02/2012 – 10/2012): Architectural design and implementation of a PCI-express NVME controller targeting the fast growing SSD market
- **10G Ethernet market** (01/2011 – 05/2012): Architectural design and implementation of a network controller device targeting latency critical applications for the 10G Ethernet market
- **Wireless Sensor Based Anti Fire System** (06/2009 – 12/2010): Fire prevention and detection system to be used in rural areas. Wireless sensor network based monitoring system

February 2005 – April 2009

Company	Montalbano Technology S.p.A.
Company Business Model	Development and Marketing of RFID smart labels and wireless sensor networks
Job Title	General Manager

Main Responsibilities	Products and technology development
	Company Strategy and organization
	Investment Planning
	Fund Raising
	Reporting to investors
	Contract negotiation with Customers and Suppliers
	Relationship with official institutions
	Human Resources coordination

I was hired in February 2005 by the founders with the mission of setting up the company from scratch starting from an innovative idea and a contract to develop a proprietary IC. I accomplished such mission by organizing the company with a structure and a strategy. I hired 10 people and built partnership with European university, research centres and industries. My work has been also decisive during the first round of capital rising which ended with Intesa-SanPaolo S.p.A acquiring a minority share of the company capital.

January 2000 – January 2005

Company	**Cadence Design Systems UK LTD**
Company Business Model	Design Services in the field of IC (Integrated circuits), SoC (Systems on Chip) and IP (Intellectual Property)
Job Title	Senior Design Engineer
List of Projects	Please refer to Annex 1
Main Responsibilities	Project Technical Leadership
	Pre-sales activities
	Project Requirement definition
	Architectural Design
	Project specification
	Design and verification

Novemeber 1996 – november 1999

Company	**Università di Genova**
Job Title	PhD Student
Research areas	Please refer to Annex 2
Main Responsibilities	Didactic activities
	Thesis supervision
	Industrial research activities in collaboration with STMicroelectronics

Education

- ***October 1999*** **Ph.D. degree** in Electrical Engineering and Computer Science from University of Genoa, discussing a dissertation on "Design and implementation of digital architectures for data transmission, data storage and data processing devices."
- ***July 1996***: "Laurea" degree certificate in Electrical Engineering from University of Genoa in July 1996 (specialization subject: **microelectronics**). Thesis title: "*Modeling and Simulation of a magnetic read and write channel*". Advisors: Prof. A. De Gloria (University of Genoa) and R. Alini (ST Microelectronics). A prize was awarded to this thesis from ST-microelectronics (Milan, Italy).

Technical skills

- Operating Systems: Windows and UNIX.
- Languages: C, Assembler.
- Hardware description languages: VHDL, VERILOG, SYSTEM VERILOG.
- Hardware verification: Specman tool set and E-language; UVM methodology, basic knowledge of System-C
- Synthesis tools: Synopsys tool set, Cadence RC.
- Simulation tools: Incisive/Xcelium, NCsim and Modelsim, Synopsys VCS.
- FPGA design tools: Synplicity Synplify, FPGA Compiler, Xilinx Flow Engine.
- Revision control tools: Synchronicity, CVS, RCS, SVN, GIT, ClearCase.

Other skills

- Mentoring and Tutoring
  faculty member
  coordinator of many thesis projects;
  wide experience of tutoring and mentoring university students;
- Leadership
  experience of management of heterogeneous teams
  used to deal with institutional investors
- Spoken and written English
  I lived and worked for 4+ years in the UK
- Good communications skills
- Good teamwork skills

Patents

- **Device for detecting impacts or vibrations** United States US 7,886,168 B2
- **Integrated solution for sensor interface for monitoring the environmental parameters by means of RFID technologies** United States US 8,035,512 B2
- **Monitoring apparatus for tanks and the like** United States US,7,760085 B2

References

Alessandra Costa Senior Vice President WW Customer Success at Synopsys, e-mail: alessandra.costa@synopsys.com
Peter Hutton Former VP Technology and Systems at ARM, Chairman at Agile Technology e-mail: Peter.Hutton@arm.com
Dave Morrison Design Engineering Director at Cadence Design Systems, e-mail: davem@cadence.com
Pete Hawkins Advanced Product Development at ARM, e-mail: pohawkins@gmail.com
Markus Dielacher Lead Principal Eng, at Infineon Gmbh
e-mail: markus.dielacher@infineon.com
Stojan Jaic Senior Staff Eng, at Infineon Gmbh
e-mail: Stojan.Jaic@infineon.com
Alexander Olbrich Senior Principal IP and solutions at Intel IMC Munich ,
e-mail: alexander.olbrich@intel.com
Fabrizio Ferrari President Aitek Srl,
Tel (+39)-010 846731, e-mail: ferrari@aitek.it
Prof. Daniele Caviglia University of Genoa, DIBE, Via Opera Pia 11a, 16100 Genoa, Italy Tel (+39)-010-3536587, e-mail: daniele.caviglia@unige.it

Publications

• A. De Gloria, D. Grosso, M. Olivieri and G. Restani “A novel stability analysis of a PLL for timing recovery in hard disk drives” IEEE Trans. on Circuits and Systems-I vol. 46 NO. 8, August 1999.
• A. De Gloria, P. Ferrari, D. Grosso, L. Puglisi and M. Olivieri “Implementation techniques for Fuzzy Theory Systems and their Applications.” Fuzzy Theory Systems Techniques and Applications, Volume 1 Edited by Cornelius .T. Leondes Academic Press (ISBN: 012-4438-70-9)
• A. De Gloria, F. Bellotti and D. Grosso "A Java based web application which addresses urban traffic problems relying on real time collected data." Software and Hardware Engineering for the 21st CenturyWord Scientific Engineering Society pp 298-305 (ISBN: 960-8052-06-8)
• A. De Gloria, F. Bellotti, D. Grosso, L.Noli and M. Olivieri " An interactive VHDL Simulator for IEEE 802.11 networks." Recent Advances in Signal Processing and Communications Century Word Scientific Engineering Society pp 239-248 (ISBN: 960-8052-03-3).
• A. De Gloria, D. Grosso, F. Sciutto and M. Oddicini, " IP cell for error correction systems in Minidisk" IEEE Trans on Consumer Electronics Vol 46 No. 1, Feb 2000 pp.58-67.
• M. Bertacchi, A. De Gloria, D. Grosso and M. Olivieri, "Semi-custom design of a IEEE 1394 compliant re-usable IC core" IEEE Design & Test Vol 17 No. 3, Jul-Sept 2000 pp.95-105.
• A. De Gloria, F. Bellotti, D. Grosso, L.Noli "WLESS - Frame: a simulation-based development environment for 802.11 stations and networks" Elsevier Science Computer Networks, Vol. 36 (Issue 5-6) August 2001 pp 625-641
• A. Rabaeijs, D. Grosso, X Huang, D. Qi “GPS Receiver Prototype for Integration into System On Chip” Trans. on Consumer Electronics vol. 49 NO. 1, February 2003.
• O. Vermesan, D. Grosso, F. Dell’Ova, C.Prior “Quo Vadis RFID Technology?” EU RFID FORUM 2007 Bruxelles March 13 and 14, 2007